



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

|                               |   |                      |
|-------------------------------|---|----------------------|
| In re Application of:         | ) |                      |
| Pierte ROO                    | ) | Examiner: M. Ghayour |
| Application No.: 09/920,241   | ) | Group Art Unit: 2631 |
| Filed: August 1, 2001         | ) |                      |
| For: APPARATUS AND METHOD FOR | ) | Date: August 9, 2005 |
| CONVERTING SINGLE-ENDED       | ) |                      |
| SIGNALS TO A DIFFERENTIAL     | ) |                      |
| SIGNAL, AND TRANSCEIVER       | ) |                      |
| EMPLOYING SAME                | ) |                      |

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In compliance with the duty of disclosure under 37 CFR § 1.56 and the requirements of M.P.E.P. § 2001.06(c), and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449 and to copies of any non-U.S. Patent or literature reference submitted herewith. It is respectfully noted that Applicants do not have copies of certain literature and non-U.S. patent documents listed on the enclosed PTO-1449 forms. Applicants will provide copies of such to the Patent Office as soon as possible. If the Examiner has not received such copies at the time of consideration of this IDS, the Examiner is respectfully requested to contact the Applicants' undersigned attorney.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

No fee is believed necessary for the submission of this Information Disclosure Statement. However, if deemed necessary, the Commissioner is authorized to charge the IDS fee of \$180.00 to Deposit Account No. 50-1710.

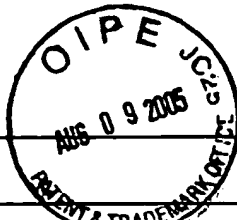
Should the Examiner have any questions, Applicant's undersigned attorney is reachable by telephone in our Washington, D.C. office at (202) 625-3547. The correspondence address of record is provided below.

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Respectfully submitted,  
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FORM PTO 1449 MODIFIED  
U.S. PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.

APPLICATION NO.

MP0088

09/920,241

**LIST OF REFERENCES CITED BY APPLICANT**

APPLICANT

Pierte ROO

DATE SUBMITTED TO USPTO: August 9, 2005

FILING DATE

GROUP

08/01/2001

2631

**FOREIGN PATENT DOCUMENTS**

| *EXAMINER<br>INITIALS | DOCUMENT NUMBER | DATE       | COUNTRY | CLASS | SUBCLASS | TRANSLATION<br>OR ABSTRACT |
|-----------------------|-----------------|------------|---------|-------|----------|----------------------------|
|                       | WO 00/28663 A3  | 05/18/2000 | Europe  |       |          |                            |
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**OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)**

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|--|---|
|  | Rao, Short Course: Local Area Networks  |
|  | Razavi, Principles of Data Conversion System Design   |
|  | Mano, Digital Logic and Computer Design   |
|  | Farjad-rad, et al., 4.5 A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly Integrated Data Communication Chip |
|  | Gotoh, et al., All-Digital Multi-Phase Delay Locked Loop for Internal Timing Generation in Embedded and/or High-Speed DRAMS         |
|  | Johnson, et al., THAM 11.2: A Variable Delay Line Phase Locked Loop for CPU-Coprocessor Synchronization                             |
|  | Sonntag, et al., FAM: 11.5: A Monolithic CMOS 10MHz DPLL for Burs-Mode  |
|  | Garlepp, et al., A Portable Digital DLL Architecture for CMOS Interface Circuits  |
|  | Lin, et al., A Register-Controller Symmetrical DLL for Double-Data-Rate DRAM  |
|  | Garlepp, et al., A Portable Digital DLL for High-Speed CMOS Interface Circuits  |
|  | Dehng, et al., Clock-Deskaw Buffer Using a SAR-Controlled Delay-Locked Loop   |
|  | Kim, et al., A Low-Power Small-Area 7.28-ps-Jitter 1-GHz DLL-Based Clock Generator  |
|  | Dehng, et al., A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm   |
|  | Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm <sup>2</sup>   |
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EXAMINER

DATE CONSIDERED

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.